Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.030”**



**.030”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: B = .004” X .004”**

**E = .004” X .006**

**Backside Potential: Collector**

**Process: 12**

**APPROVED BY: DK DIE SIZE .030” X .030” DATE: 11/17/21**

**MFG: FAIRCHILD THICKNESS .007” P/N: 2N1893**

**DG 10.1.2**

#### Rev B, 7/19/02